2121 #4 BT
02-7-03

D'Arcy 13-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): P.G. D'Arcy et al.
Case: 13-1
Serial No.: 10/028,453
Filing Date: December 24, 2001
Group: 2121
Examiner: To Be Assigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature: Lisa L. Vulpis Date: January 28, 2003

Title: High Speed Add-Compare-Select Operations for Use in Viterbi Decoders

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants' attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying Form PTO-1449. A copy of each listed document is enclosed.

U.S. Patent Documents

1. U.S. Patent No. 5,559,837 issued on 9/24/96 to Blaker et al.
2. U.S. Patent No. 5,537,445 issued on 7/16/96 to Blaker et al.
3. U.S. Patent No. 5,533,065 issued on 7/2/96 to Blaker et al.
4. U.S. Patent No. 5,490,178 issued on 2/6/96 to Blaker et al.

Other Documents

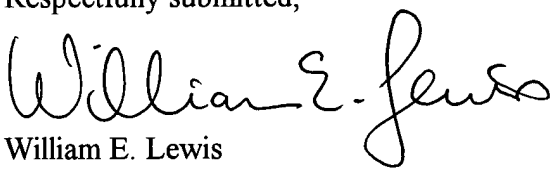
1. A. Weinberger, "4:2 Carry Save Adder Module," IBM Technical Disclosure Bulletin, Vol. 23, pp. 3811-3814, January 1981.

2. G. Fettweis et al., "High-Rate Viterbi Processor: A Systolic Array Solution," IEEE Journal of Selected Areas in Communication, Vol. 8, pp. 1520-1534, October 1990.

It is believed that there is no fee due in conjunction with the filing of this Information Disclosure Statement. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Ryan, Mason & Lewis, LLP Deposit Account No. 50-0762** as required to correct the error.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,



Date: January 28, 2003

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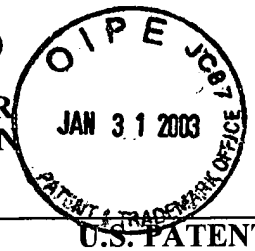
FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT



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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
___	5,559,837	9/24/96	Blaker et al.		
___	5,537,445	7/16/96	Blaker et al.		
___	5,533,065	7/2/96	Blaker et al.		
___	5,490,178	2/6/96	Blaker et al.		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES	NO

OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

___ 1. A. Weinberger, "4:2 Carry Save Adder Module," IBM Technical Disclosure Bulletin, Vol. 23, pp. 3811-3814, January 1981.

___ 2. G. Fettweis et al., "High-Rate Viterbi Processor: A Systolic Array Solution," IEEE Journal of Selected Areas in Communication, Vol. 8, pp. 1520-1534, October 1990.

Examiner _____ Date Considered _____

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.